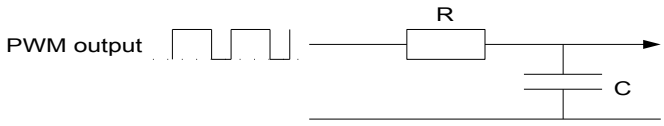
Simple PWM DAC design considerations

Many single chip microprocessors include a PWM (Pulse Width Modulation) output and its tempting to use this as a DAC (Digital to Analogue Converter) for generating waveforms etc. – however there are a few design aspects to consider before doing so.

PWM output is a rectangular waveform of constant frequency where the duty cycle (the ratio of on to off) is varied. In order to use the PWM as a DAC the output must be passed through a low pass filter (LPF) to remove the PWM fundamental frequency and average the output voltage.

The simplest form of low pass filter is a RC network - which gives a 1st order filter. More complex filters can be used (and will improve results) but require additional circuitry. One should consider the worth of the additional circuitry required vs the use of a real DAC.



Lets examine DAC quantization step size in terms of dBs:

Number of DAC bits	Quantization step (voltage)	in terms of dBs (power)
1	1/2	6dB
2	1/4	12dB
3	1/8	18dB
4	1/16	24dB

In general we get a figure of 6dB per DAC bit. In order to use a PWM DAC properly we need to set the LPF cutoff frequency such that the residual voltage ripple is less than the quantization step size of the DAC. Here we will set the ripple to half the quantization step size.

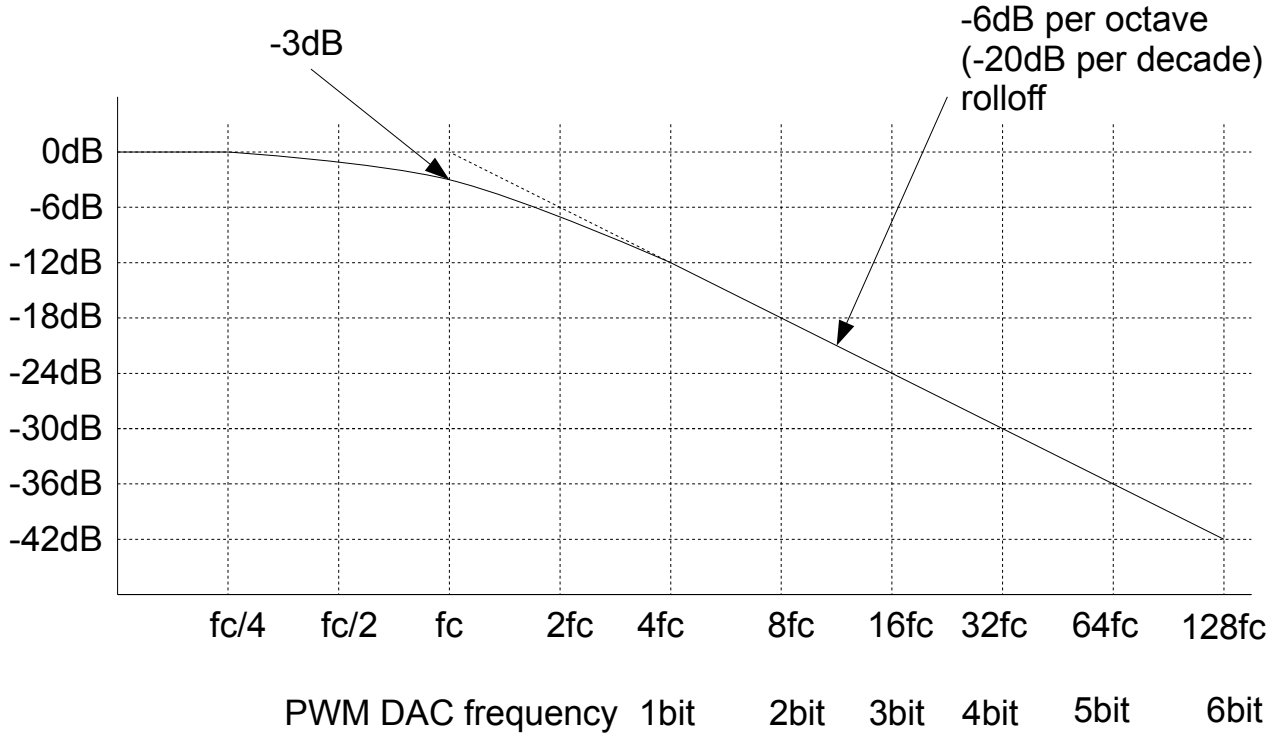
A simple RC (1st order) filter has a cutoff frequency of $1 / (2\pi RC)$ and a roll off of 6dB (power) per octave (a halving or doubling of frequency). We must set the LPF cutoff frequency low enough that the PWM fundamental is filtered to a value less than the quantization step – we can see from the above that for every DAC bit we introduce we must half the RC filter cutoff frequency.

If we make PWM ripple half the amplitude of the quantization step size we need to set the LPF one further octave less than the PWM frequency (PWMfreq). Hence:

$$\text{LPF cutoff frequency} = \text{PWMfreq} / 2^{(1 + \text{DACbits})} = 1 / (2\pi * RC)$$

$$RC = 2^{\text{DACbits}} / (\pi * \text{PWMfreq})$$

We can improve the frequency response of the DAC (i.e. increase the LPF cutoff frequency) by increasing the PWM frequency – however the upper limit of the PWM frequency is typically set by the processor clock and the number of PWM bits required. Note: the downside of increasing the processor clock is that it drives up the current consumption.



1st order low pass filter characteristics and choice of DAC frequency.

Lets look at some examples assuming a 4MHz processor clock:

PWM bits	PWM frequency	LPF cutoff frequency
10	3906.25 Hz (4MHz / 1024)	1.9Hz
9	7812.5Hz	7.6Hz
8	15625Hz (4MHz / 256)	30.5Hz
7	31250Hz	122Hz
6	62500Hz (4MHz / 64)	488Hz
5	125000Hz	1.95KHz
4	250000Hz (4MHz / 16)	7.81KHz

indicating that only 4 or 5 bit DAC resolution is achievable at voice frequencies with a 4MHz clock.

Using as 16MHz processor clock:

PWM bits	PWM frequency	LPF cutoff frequency
10	15625 Hz	7.6Hz
9	31250Hz	30.5Hz
8	62500Hz	122Hz
7	125000Hz	488Hz
6	250000Hz	1.95KHz
5	500000Hz	7.81KHz
4	1000000Hz	31.25KHz

Showing that a quadrupling of processor speed only results in a single bit DAC improvement. This is because we need half of the frequency increase to provide the extra octave of 1st order LPF filtering needed for the extra DAC bit and the other half is used to increase the PWM resolution by 1 bit.

Using a 20MHz processor clock:

PWM bits	PWM frequency	LPF cutoff frequency
10	19.5KHz	9.5Hz
9	39KHz	38.1Hz
8	78KHz	153Hz
7	156KHz	610Hz
6	312KHz	2.4KHz
5	625KHz	9.8KHz
4	1.25MHz	39KHz